

EDA Alert article:

1. Viewpoint -- Exclusive to EDA Alert

Electronic System-Level Design Is Ready: Are You?

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Does it make sense to spend six months designing a complex system architecture only to throw it away and start all over again in RTL? Of course, you'll then have to do from one to three chip re-spins to finally get it right. Why do so many companies think that this is "normal," "the way it has always been" and "inevitable," like gravity or the coming of winter?

Architects and designers should be having a fit over this waste of their talent and time, and immediately demand electronic system-level (ESL) design platforms. While ESL is still young, the last few years have seen truly production-worthy tools come to market. For example, today it is both possible and productive to model complex SoC architecture in software. This will create a virtual system prototype that you can use to begin hardware and software development in parallel and enable true co-verification. So why are so few people taking advantage of this next level of design abstraction?

The problem is not that there's a lack of technology; it's that people are notoriously slow to adopt new methods and tools. One wag once recommended that people should "stop waiting for the future and become part of the 10% that are already living in it." That's very true. With every advance, 10% of the population always leads the rest by five to ten years. In the case of EDA tools, we observed this phenomenon with the adoption of simulation and formal verification. Our great-grandparents observed the change from horses to automobiles and currently, as 10% of the population moves happily to taking digital pictures with their cell phones, the rest of us still run to the drug store to have pictures developed that will end up in a box in the garage. The good news is that you don't have to be part of the 90% who eventually catch on -- you can be among the 10% operating in the future today.

The first step is to take a look at the ESL solutions with a successful track record in production environments. Solutions should have the following attributes:

- * Actually have been used in production for multiple years.
- * Successfully have taped out real chips and brought real systems to market.
- * Reduced the need for point tools (i.e., the solution can be used by architects as well as software and/or hardware designers).
- * Facilitated hardware/software co-design and co-verification.
- * Improved technical communications between team members, customers and suppliers, and geographically distributed development teams.
- * Supported architecture and design reuse at the system and block level.
- * Helped design teams achieve significant, measurable reduction in cost and time-to-market after users become proficient.

Once you've done your technical assessment, projected and compared cost and time reductions, and picked your favorite, then set up a pilot or shadow project and get going. Yes, be rigorous; yes, measure actual results; yes, factor in the cost of retraining and retooling. But for heaven's sake, get moving. ESL is ready. Are you?

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