

VaST Systems Technology Corporation

# Inaugural Technical Advisory Board Meeting

## Objectives & Schedule & Summary

TAB & Meeting	0900-1600: Sunday, 12 June 2005  President B Room, Radisson Maingate Hotel  1850 S. Harbor Blvd., Anaheim, CA 92802  Tel: +1-714-750-2801
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### 1. Objectives of the TAB Meeting

To engage a gathering of expert in considering a number of hairy and significant issues arising in the multi-technology discipline of Embedded Electronic Systems Engineering, including:

- i. The effect of Virtual System Prototyping on the Systems Engineering process. What is the effect of incorporating Virtual System prototyping into the conventional sequential Systems Engineering process?
- ii. Executable System Specifications: What are they? Can they be mapped onto physical realizations?
- iii. How the Systems Engineering process can be driven empirically to effect the:
  - o Optimization of Executable Specifications leading to optimal physical systems
  - o The use of mappings (such as, specifications → concurrent systems, s/ware → h/ware) in the optimization process.
- iv. Standards for Transaction Level interfacing and interconnection: What does it buy? Who will be converts?

## 2. The Inaugural TAB Program

Time	Working Session	Activity
0900-0910		Welcome, introductions and CEO note
0910-0930	0	Outline & Objectives of the VaST TAB Sponsored Day on Systems Engineering
0930-1050	1	<p><b>The Impact of Virtual System Prototyping on the Systems Engineering Process</b></p> <ul style="list-style-type: none"> <li>Frank Winters, Delphi: <i>Virtual Prototyping in Automotive Electronics</i> [<a href="http://vastsystems.com/docs/DesignProcessChangesEnablingRapidDevelopment.pdf">http://vastsystems.com/docs/DesignProcessChangesEnablingRapidDevelopment.pdf</a>]</li> <li>Carsten Mielenz, Infineon: <i>Virtual Prototyping in Mobile Systems</i> [<a href="http://vastsystems.com/docs/VirtualPrototyping1.pdf">http://vastsystems.com/docs/VirtualPrototyping1.pdf</a>]</li> <li>Discussion: Integrating VS Prototyping in the Engineering Process Design Flow</li> </ul>
1050-1110		AM Tea / Coffee
1110-1240	2	<p><b>System Specification and Mapping to Multiple and Distributed Processing Architectures on a Chip</b></p> <ul style="list-style-type: none"> <li>Chuck Pilkington, ST Micro: <i>The MultiFlex Approach to System Specification &amp; Mapping</i> [<a href="http://vastsystems.com/docs/The%20MultiFlex%20Approch%20to%20System.pdf">http://vastsystems.com/docs/The%20MultiFlex%20Approch%20to%20System.pdf</a> ]</li> <li>Wayne Wolf, Princeton: <i>Cool Architectures</i> [<a href="http://vastsystems.com/docs/Cool%20Multiprocessors_Distribute.pdf">http://vastsystems.com/docs/Cool%20Multiprocessors_Distribute.pdf</a>]</li> <li>Discussion: Higher Complexity Systems: Specification and Mapping to Architectures</li> </ul>
1240-1330		Lunch
1330-1500	3	<p><b>Modeling Standards and the Quantitative Optimization of Architectures</b></p> <ul style="list-style-type: none"> <li>The Need for Modeling Standards [<a href="http://vastsystems.com/docs/The%20Need%20for%20Modeling%20Standards06.12.2005.pdf">http://vastsystems.com/docs/The%20Need%20for%20Modeling%20Standards06.12.2005.pdf</a>]</li> <li>Graham Hellestrand, VaST: <i>Empirical Systems Architecture</i> [<a href="http://vastsystems.com/docs/EmpiricalSystemsArchitecture20050722Pub.pdf">http://vastsystems.com/docs/EmpiricalSystemsArchitecture20050722Pub.pdf</a>]</li> <li>Discussion: Building Optimal Architectures &amp; the Role of Standards</li> </ul>
1500-1515		PM Tea / Coffee
1515-1600	4	<p>Summary and Actions:</p> <ul style="list-style-type: none"> <li>Transaction Level Interfacing</li> <li>Specification and Mapping</li> <li>Executable Specification</li> </ul>

### 3. Summary of the Discussions

The First Session - **The Impact of Virtual System Prototyping on the Systems Engineering Process** - had 2 speakers. Frank Winters and Carsten Mielenz presented the use of high performance, timing accurate Virtual System Prototypes (VSP – systems constructed from under-development and production quality software executing on models of processors interfaced, via models of buses and bus bridges, to models of digital and analogues electronic, RF, mechanical and abstract devices) in the automotive and wireless industries.

In automotive, VSPs are used pre-silicon - to overlap the software and hardware development phases of modern controllers used in cars and post-silicon - due to the impact of the major advantages provided by controllability, observability and defensible usage of models, on the efficiency and effectiveness of the embedded software development process. The reasons for the use of VSPs in automotive together with the successful development of a *restraint system* was discussed by Frank.

In wireless, VSPs enable full software to be ported and developed pre-silicon with major impact on time-to-market of mobile phones and base-stations. A profound usage of VSPs is their use in developing *optimal* architectures that then enable pre-silicon software development and drive hardware design. Carsten provided a technical overview of virtual prototyping and its use in developing a mobile handset with a complex protocol stack, still and video picture and audio processing, and extensive user capabilities.

Each speaker provided cross references to the other's presentation and a combined summary might be:

- Complexity of Control Systems in Wireless and Automotive Products Will Continue to Grow.
- Understanding and Developing Distributed Control Systems Is a Major Challenge for the Future.
- Pressures to Decrease Development Cycles and Cost Will Continue While Quality Expectations Increase.
- Cycle Accurate, High Performance Simulations of Virtual Prototypes, Prior to Physical Systems Enables Rapid Development.

The second Session - **System Specification and Mapping to Multiple and Distributed Processing Architectures on a Chip** – also had 2 speakers. Chuck Pilkington discussed strategies for mapping of various types of algorithmic concurrency (coarse concurrency – operating system processes/tasks, fine concurrency – short threads, instruction concurrency – VLIW, SIMD) to underlying architectures that effectively support them. These architectures incorporated subsystems that were network-on-chip connected, with the subsystems typically being closely coupled. Wayne Wolf discussed the use of multiple and distributed processors in solving several computationally complex problems. Distributed systems on a chip are connected conveniently using Networks on Chip – either conventionally bus-based or crossbar-based depending on bandwidth and silicon area constraints. The mapping of various problems to multiple and distributed architectures was studied under simulation with result indicating configurations of interconnect that enabled desired tradeoffs of communication bandwidth and required computational performance to be achieved.

The Third Session - **Modeling Standards and the Quantitative Optimization of Architectures** – was truncated due to time constraints. The presentation on **Modeling Standards** made the case for enabling interoperability of models between vendor systems, perhaps based on SystemC and a TLM standard - a necessary step to encourage the proliferation of models and tools. The content of the intended final presentation is captured in the paper presented at EmSoft2005.

The TAB concluded its work with useful discussion of several topics:

- Transaction Level Interfacing
- Specification and Mapping
- Standardization